Briefing to the ESSAAC Technology Subcommittee (TSC)

on

Radar/Radiometer Processing Technology Roadmap

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Background

- Instrument data processing technology is currently primarily ground-based
  - Data processing needs far outstrip on-board capabilities
  - Instruments are designed with output data streams that fit within affordable downlink and on-board storage capabilities
  - Some basic processing in FPGAs and ASICs has been flown for NASA instruments
  - Commercial satellites often use expensive special purpose ASICs for processing (multiplexing, filtering, beam-forming)
- Future science instruments will produce prodigious amounts of data
  - Distributed array antennas with many sampled phase centers
  - Desire for synoptic coverage of very wide areas at high resolution
  - Desire for autonomous decision making based on observations

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Enabling vs. Enhancing

- On-board processing is *enabling* if
  - The data collected could not affordably be downlinked and processed (e.g. multi-aperture beam synthesis)
  - The instrument configuration depends on real-time calculations (e.g. active wavefront control, RFI rejection)
- On-board processing is *enhancing* if
  - Data could be processed either on-board or on the ground, with benefits to processing on board (e.g. cost reduction)
- Scientists and instrument designers rarely consider enabling processors as part of their vision
  - Processing technology is not often instrument specific
  - Designers do not control processing technology developments
  - Downlinks and storage capabilities continuously improve

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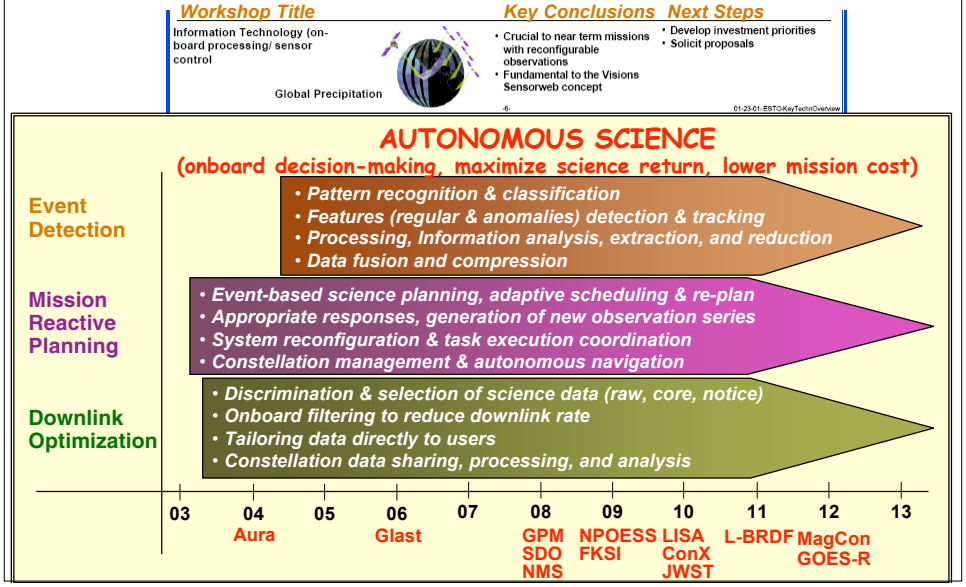
OBP Application Roadmap

NASA Earth Science Enterprise, Technology Planning Workshop (Jan 01)

Workshop Title		Key Conclusions	Next Steps
Information Technology (on-board processing/ sensor control	Global Precipitation	• Crucial to near term missions with reconfigurable observations • Fundamental to the Visions Sensorweb concept	• Develop investment priorities • Solicit proposals



Mapping Measurement Scenarios to Processing Technology

- Processing Group (Dan Evans, Paul Rosen) followed same flow-down of requirements as radar/radiometer hardware elements
  - Science focus area requirements
  - Measurement scenarios meeting science requirements
  - Role of on-board processing in accomplishing these measurements
  - Processing capabilities challenges defined
- General Observations
  - SAR instruments generally require large on-board storage capacity, particularly interferometric applications
  - Multi-aperture systems require high throughput processors and data links
  - Passive systems need high bandwidth low precision digital hardware
  - Active systems need medium bandwidth high precision digital hardware
  - As system migrate to higher orbits, radiation hardening and fault tolerance become important considerations

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Processing technology development needs for NASA ESE science focus areas

- Large rad-hard on-board storage capability
  - Measurements in virtually all focus areas
- Real-time on-board processing
  - Polarimetric and Interferometric measurements in solid Earth and Carbon Cycle focus areas
  - Real-time tracking of hurricanes and other weather
- Radiation Hard Processors
  - Measurements acquired from orbital altitudes exceeding 2000 km from all focus areas
- Processing Algorithms
  - Real-time algorithms for topography incorporating state information
  - High-earth orbit curvature effects in SAR processing
  - Mapping of standard algorithms to real-time environment
  - RFI Mitigation
- High Performance A/D and digital receivers
  - Digital-beamforming processors
  - High-performance, low-power A/D converters for radars
  - Modular digital receivers
  - High-rate low-precision A/D converters for radiometers

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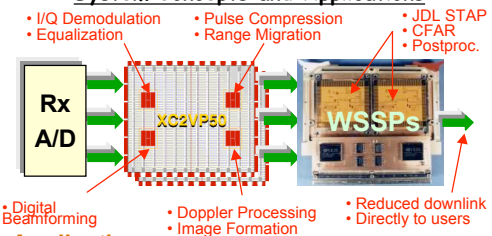
Example OBP Technology Need

Description of Technology and Issues

- ***Real-Time Heterogeneous Fault-Tolerant High-Performance Architecture for SAR & STAP Processing***
  - FPGA front-end: fixed-point regular operations
  - Microprocessor back-end: adaptive floating-point alg.
  - Fault-Tolerant architecture: multi-level dynamic TMR
- ***Current state of the art***
  - Non real-time ground processing
- ***Technical Challenges:***
  - Space qualified implementation
  - Architecture optimization
  - High throughput, scalability and flexibility
- ***Enabling Innovation:***
  - Fast large-memory massive-parallel FPGA technology
  - Rad-tolerant commercial-fab low-power μprocessors
  - Integrated tools and system-on-chip (SoC) technology

System Concepts and Applications



Applications

- **NASA: Sensor Web, GESS, UAVs, CLPM, other space exploration missions**
- **AF: MIT, SAR, DTED FEP, UAV's, inceptors, other satellites**

Personnel, Skills, and Commitments

- ***JPL: SAR/DBF/FT FPGA Design***
  - Charles Le, algorithm specification and development
  - Biren Shah, SAR design and implementation
  - Mark Fischman, DBF design and implementation
  - Winston Fang, FT design and implementation
- ***AFRL: STAP programmable design***
  - Microprocessor design, real-time programming
  - System integration
- ***Synergies:***
  - Boeing's AESOP (Architecture Enhanced SBR OBP)
  - JPL's MCD (Maximum Convolutional Decoder, DSN)

Deliverables

- ***SAR:*** synthesizable (RTL) model, bit file of range compression module on Xilinx's Virtex-II FPGA chip.
- ***DBF:*** post place-and-route bit file for Xilinx's Virtex-II.
- ***FT:*** schematic and simulation of the FT system arch.
- ***Documents:*** design & implementation, testing results.

Current TRL Status	Start TRL	End TRL
Components (FPGA, WSSP)	3	4
Subsystems (FT, comm. network)	2	3
System (interface, integration)	2	3

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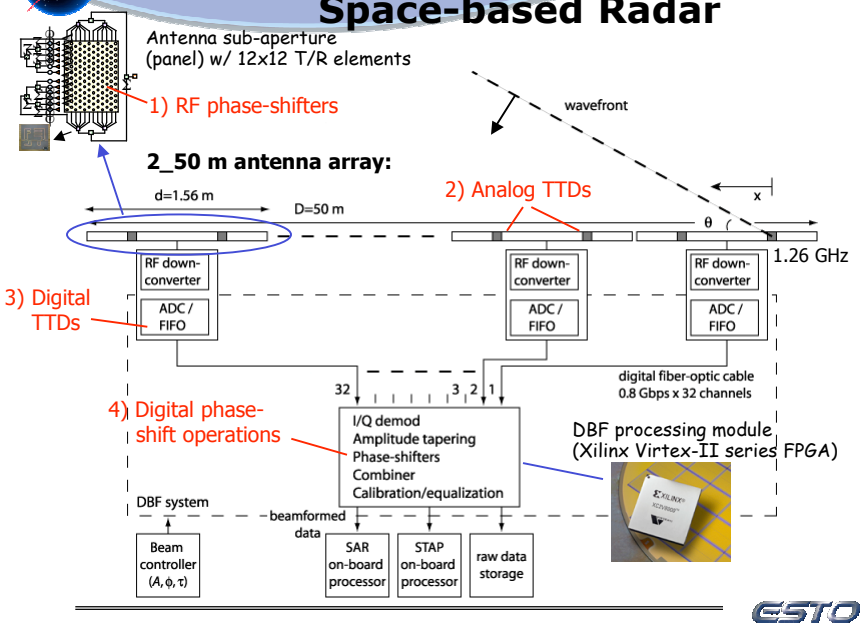
Example Beamforming approach in Space-based Radar



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Example Metrology/Calibration Technology Need

Description of Technology and Issues

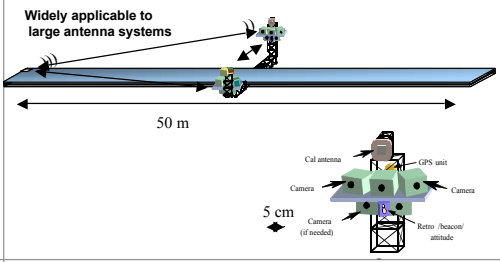
Calibration and Metrology System for large deployable array
- Supports active array operations
- Calibrates array to 4 mm element-to-element path delay

Current state of the art
- SRTM two-point position/attitude measurement system

Enabling Innovation:
- calibration circuitry in T/R, calibration towers, multi-target metrology, calibration processor

Technical Challenges:
- real-time calibration control

System Concept



Personnel, Skills and Commitments

Dalia McWatters, Radar Systems, 0.4
Adam Freedman, Radar Metrology, 0.5
Vaughn Cable, Electromagnetics for RF cal, 0.3
Thierry Michel, Antenna Simulations, 0.1

Other Assumptions

Components are developed by other tasks to be flight qualified

Applications
- NASA: L-band SAR/InSAR/ATI
- AF: L-band AMTI/SAR/FOPEN
- DARPA: ISAT

Current TRL Status	Start TRL	End TRL
Components	N/A	N/A
Subsystems this year	2	3
System this year	2	3

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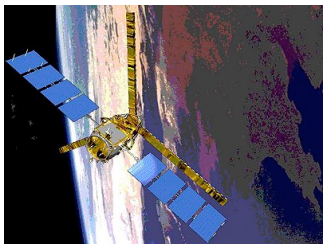
2-D STAR Processor Technology Needs

Description of Technology and Issues

Sparse aperture radiometer array

Technical Challenges:
- 1-bit A/D Converters for cross-correlator inputs
- 2-bit A/D converters for self-correlation (power)
- 1-bit high speed cross-correlation processors
- High-speed data links for transfer of data to correlation processor

System Concept



Personnel, Skills and Commitments

Processing technology development modestly funded at the component level at GSFC and various universities

Applications
- Soil moisture
- Sea salinity
- Winds
- Snow-water equivalent

- Presently low TRL (2-3)

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Processing Challenge Histogram
(Measurement Scenarios Supported)

• Large Data Storage	21
• Processing Algorithms	8
• High Performance RHP	21
• High Performance A/D Digital Receivers	21
• Real-time On-board Processing	34
• 1-bit A/D for Radiometry	9
• 2-bit A/D for Radiometry	9
• High-bandwidth Data Links (Interior to Instrument)	13
• Digital RFI Mitigation	1
• On-board High-rate Digital Signal Distribution	4
• High-speed, High-resolution, Digital Spectrometers for Sounding	3
• Combined Passive/Active Processing, Distribution	1
• Massively Parallel 1-Bit Cross-correlators for Radiometry	9

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Processing Challenges Overview

Where we are now	Where we plan to be
Limited on-board storage requiring data transmission when storage limits exceeded	>one terabit radiation hardened on board storage with 100 MHz clock rate and < 100 W access power
Processing algorithms a variety of applications do not currently exist	Position and Velocity, Topography, Polarimetric SAR, MEO SAR, and Rain Profile Algorithms
Transmission to the ground and subsequent ground processing when necessary	A High Performance Radiation Hardened Processor for harsh radiation environment
Conventional radar receivers and A/D converters	Multi-channel digital receiver/beamformer
Intensive radar processing performed on ground	Real-time on-board SAR and InSAR processing
Initial work on 1 or 2 bit A/Ds for STAR	200 MHz, 10mW ASIC Chip
Limited bandwidth data links interior to instrument	High-bandwidth data links sufficient for STAR
No existing digital RFI	Data cleansed by means of digital processing
No existing on board high rate digital distribution	High-rate data bus in deployed STAR instrument ~30 Gbps channel capacity; ~20 W per channel
Sounder processing performed on ground	Digital autocorrelator or polyphase spectrometer 4-8 GHz bandwidth, a few Watts/spectrometer), & radiation hardening
1-bit cross-correlators for STAR under development	10k threshold 90k objective 1-bit cross-correlations per ASIC; 0.25 mW threshold, 0.1 mW target 220 MHz clock

2004 ~ 2014 or earlier

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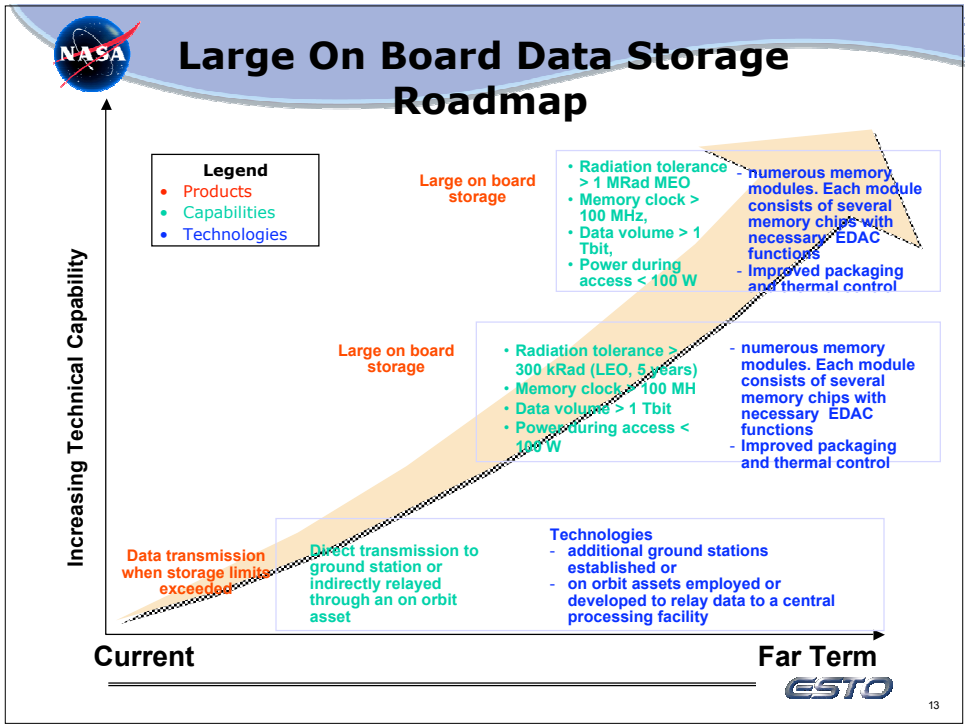
Large On Board Data Storage Roadmap
Legend
Products
Capabilities
Technologies
Large on board storage
• Radiation tolerance > 1 MRad MEO
• Memory clock > 100 MHz,
• Data volume > 1 Tbit,
• Power during access < 100 W
- numerous memory modules. Each module consists of several memory chips with necessary EDAC functions
- Improved packaging and thermal control
Large on board storage
• Radiation tolerance > 300 kRad (LEO, 5 years)
• Memory clock > 100 MH
• Data volume > 1 Tbit
• Power during access < 100 W
- numerous memory modules. Each module consists of several memory chips with necessary EDAC functions
- Improved packaging and thermal control
Data transmission when storage limits exceeded
Direct transmission to ground station or indirectly relayed through an on orbit asset
Technologies
- additional ground stations established or
- on orbit assets employed or developed to relay data to a central processing facility
Increasing Technical Capability
Current
Far Term
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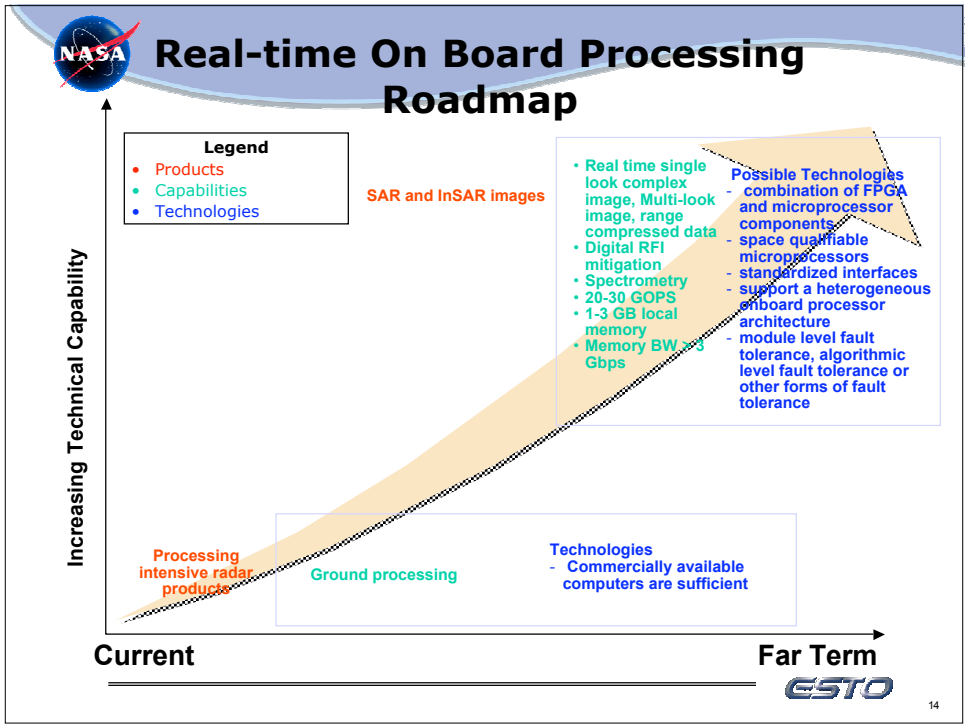
Real-time On Board Processing Roadmap
Legend
Products
Capabilities
Technologies
SAR and InSAR images
• Real time single look complex image, Multi-look image, range compressed data
• Digital RFI mitigation
• Spectrometry
• 20-30 GOPS
• 1-3 GB local memory
• Memory BW ~3 Gbps
Possible Technologies
- combination of FPGA and microprocessor components
- space qualifiable microprocessors
- standardized interfaces
- support a heterogeneous onboard processor architecture
- module level fault tolerance, algorithmic level fault tolerance or other forms of fault tolerance
Processing intensive radar products
Ground processing
Technologies
- Commercially available computers are sufficient
Increasing Technical Capability
Current
Far Term
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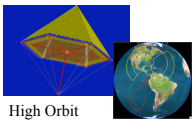
Integrated Radar/Radiometry Processing Challenge Roadmap (2004-2015)

Current ESTO funding
Future ESTO funding

Rad-hard On-board Storage — 2004 – 2006
1 Tbit rad-hard storage, 100 MHz clock, < 100 W access power

Processing Algorithms — 2010
Real-time algorithms for topography, digital RFI and polyphase filters, MEO SAR, off-nadir Rain Profiles

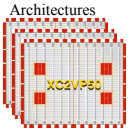


High Orbit Rad-hard applications

Rad-Hard On-board Processors — 2009
Rad-hard processors for MEO radiation environment

Real-time On-board Processing — 2009
Real-time processing for digital RFI mitigation, spectrometry, SAR and InSAR, 20-30 GOPS, 3 Gbytes cache memory

Fault Tolerant FPGA Architectures

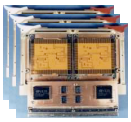


Multi-channel Digital Receivers and Beamforming — 2012
FPGA and/or ASIC based 4-12 bit digital beamforming at 2 GHz rates

1-3 bit A/D Converters
3 GHz BW, 2 GHz clock, 5mW, 1 mV Q_{in} ASIC Chip

1-bit Cross-correlators — 2014
10k threshold 90k objective 1-bit cross-correlations per ASIC; 0.25 mW threshold, 220 MHz clock

High Bandwidth Data Links — 2014
Over copper: >1 Gb/s data link, <20 mW DC power, >3-meter haul.



General Purpose DSP/Processors for Space

High Bandwidth Data Distribution — 2014
30 Gbps channel capacity; 20 W per channel

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